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(54) Title: APPARATUS FOR ITERATIVE HARD-INPUT FORWARD ERROR CORRECTION DECODING

(57) Abstract: An apparatus for iterative hard-decision forward error correction decoding is described. A method comprises a binary receiver to convert an optical signal to an electrical signal, the electrical signal having a set of information symbols and a set of redundancy symbols, the set of redundancy symbols generated by different forward error correction (FEC) encoding schemes, and a first of a plurality of decoders coupled with the binary receiver and the plurality of decoders coupled together, each of the plurality of decoders to decode the set of information symbols with the set of redundancy symbols in accordance with the different FEC encoding schemes.

APPARATUS FOR ITERATIVE HARD-DECISION FORWARD ERROR CORRECTION DECODING

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The invention relates to the field of communications. More specifically, the invention relates to error correction in communications.

Background of the Invention

[0002] In communication networks, forward error correction (FEC) is used to protect transmitted information from impairments that occur while being transported in a transmission system. In the case of algebraic block codes (e.g. the Reed Solomon code), redundancy symbols are added to the information symbols before transmission of a block of symbols. A network element that receives the transmission can correct transmission errors as long as the number of corrupted symbols does not exceed a certain threshold given by the special construction of the code.

[0003] An alternative to algebraic coding is iterative coding. Iterative coding algorithms have been developed for correction of streams of transmitted information where scalar information representing the reliability of a received symbol of the stream of transmitted information is available. These iterative coding algorithms are also referred to as soft-decision algorithms.

[0004] However, soft-decision coding techniques generally do not apply in optical networks where high transmission rates interfere with the ability to generate reliability information for received symbols. Moreover, soft-decision coding algorithms tend to have relatively poor performance for streams of transmitted information with low probability of bit errors after correction, which occurs in optical networks.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The invention may best be understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0006] Figure 1A is a diagram of exemplary network elements according to one embodiment of the invention.

[0007] Figure 1B illustrates input bit error rate (BERi) versus output bit error rate (BERo) with three exemplary encoding schemes with 25% of FEC related overhead added to the exemplary signals while transmitted according to one embodiment of the invention.

[0008] Figure 2 is a an exemplary flowchart for encoding data according to one embodiment of the invention.

[0009] Figure 3A is a diagram illustrating exemplary interleaving of two code classes in a matrix according to one embodiment of the invention.

[0010] Figure 3B is a diagram illustrating exemplary interleaving of a third code class into the matrix of Figure 3A according to one embodiment of the invention.

[0011] Figure 3C is a diagram illustrating an alternative exemplary interleaving of two code classes according to one embodiment of the invention.

[0012] Figure 4 is a flow chart for the decoding of data according to one embodiment of the invention.

[0013] Figure 5 is a diagram of components of a line card of a network element for according to one embodiment of the invention.

[0014] Figure 6A is a diagram illustrating an exemplary embodiment of the invention of the iterative decoder 505A of Figure 5 according to one embodiment of the invention.

[0015] Figure 6B is a diagram illustrating an exemplary embodiment of the invention of the iterative decoder/dewrapper and encoder/wrapper 509 according to one embodiment of the invention.

[0016] Figure 7 is a diagram illustrating an iterative decoder with backward annotation according to one embodiment of the invention.

[0017] Figure 8 is a diagram illustrating an iterative decoder with forward annotation according to one embodiment of the invention.

DETAILED DESCRIPTION OF THE DRAWINGS

[0018] In the following description, numerous specific details are set forth to provide a thorough understanding of the invention. However, it is understood that the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the invention.

[0019] Figure 1A is a diagram of exemplary network elements according to one embodiment of the invention. In Figure 1, a network element 101 is coupled with a network element 103. A wrapping/encoding unit 107, which will later be described in more detail herein, in the network element 101 receives data 105. The data includes a set of information symbols. One or more bits may represent each of the information symbols. The wrapping/encoding unit 107 adds overhead space to the data 105 (referred to as wrapping). The wrapping/encoding unit 107 initially fills part of the overhead space with administrative information. The administrative information may include patterns for code synchronization. The wrapping/encoding unit 107 then fills the remaining overhead space in the data 105 with redundancy symbols derived from the information symbols of the data 105. The redundancy symbols are members of interleaved code classes, which are later described in more detail herein. The wrapping/encoding unit 107 passes the wrapped data 106 to an optical transmitter 109. The optical transmitter 109 converts the wrapped data 106 from an electrical signal to an optical signal 108. The optical transmitter 109 then transmits the optical signal 108 from the network element 101 to the network element 103. In one embodiment of the invention, the wrapping/encoding unit 107 and the optical transmitter 109 are separate units. In an alternative embodiment of the invention, the wrapping/encoding unit 107 and the optical transmitter 109 are a single unit.

[0020] An optical receiver 111 in the network element 103 receives the optical signal 108. The optical receiver 111 converts the optical signal 108 into an electrical signal that is received wrapped data 110 and passes the received wrapped data 110 to a multiple code class iterative decoding unit 113. The received wrapped data 110 is the same as the wrapped data 106 if the wrapped data has not been impaired. For the purposes of this illustration, it is assumed that the received wrapped data 110 is the wrapped data 106 with impairments.

[0021] The multiple code class iterative decoding unit 113 processes the received wrapped data 110 with the added redundancy symbols to generate processed wrapped data 112. The multiple code class iterative decoding unit 113 passes the processed wrapped data 112 to a de-wrapping unit 115. The multiple code class iterative decoding unit 113 and the de-wrapping unit 115 will later be described in more detail herein.

[0022] The de-wrapping unit 115 removes the administrative information and overhead space formerly carrying the redundancy symbols from the processed wrapped data 112. The de-wrapping unit 115 then outputs data 117, which is identical to the original data 105, except for those locations in the data 117 with uncorrectable error constellations. The difference between the original data 105 and the output data 117 is referred to as output error rate. Various embodiments of the invention may implement the optical receiver 111, the multiple code class iterative decoding unit 113, and de-wrapping unit 115 differently. The optical receiver 111, the multiple code class iterative decoding unit 113, and de-wrapping unit 115 may be a single unit; the optical receiver 111 and the multiple code class iterative decoding unit 113 may be a single unit that is separate from the de-wrapping unit 115; or the multiple code class iterative

decoding unit 113 and the de-wrapping unit 115 may be a single unit that is separate from the optical receiver 111.

[0023] Applying hard-decision FEC to optically transmitted data with interleaved code classes reduces output bit error rate.

[0024] Figure 1B illustrates input bit error rate (BERi) versus output bit error rate (BERo) with three exemplary encoding schemes with 25% of FEC related overhead added to the exemplary signals while transmitted according to one embodiment of the invention. The BERi is the probability of a single bit transmission error whereas the BERo is the probability of a single bit being corrupted after decoding a data based on an Averaged White Gaussian Noise model. The dotted line labeled "RS (255, 205)" illustrates the performance of a single stage Reed-Solomon encoding scheme. The dashed line labeled "Simple product decoding" illustrates the performance of a simple Reed-Solomon based block product encoding scheme with optimized code parameters. The solid line represents the performance of an encoding scheme implementing an iterative hard decision decoding of two interleaved code classes with two iterations. As illustrated in Figure 1B, the encoding scheme that implements iterative hard-decision decoding of interleaved code classes outperforms the other exemplary encoding schemes at input BERs that typically occur in optical transmissions.

[0025] Figure 2 is a an exemplary flowchart for encoding data according to one embodiment of the invention. At block 201, an encoding scheme is selected. Selecting an encoding scheme includes selecting which forward error correction (FEC) encoding procedure is to be used (e.g., BCH encoding, Reed-Solomon encoding, etc.) and selecting the parameters to be used with the encoding algorithm. In one embodiment of the invention, the set of parameters and procedures are predefined. In alternative embodiments of the invention, the parameters and encoding procedure are retrieved

from memory, a user selects the parameters and the encoding procedure, the encoding procedure is selected at random from a set of encoding algorithms and each encoding algorithm has a predefined set of parameters, a set of parameters are selected from a predefined set of parameters at random to be used with a predefined encoding procedure, the parameters and/or the encoding procedure are selected from different parameters and/or encoding procedures stored on a wrapping/encoding unit and/or a separate storage unit, etc..

[0026] At block 203, data is received. At block 205, the data is processed with the selected encoding scheme to generate a set of code words (i.e., the data along with redundancy data) of a first code class. The term code class refers to all code words generated with a certain encoding procedure and a certain set of parameters. While in one embodiment of the invention different code classes are generated by the same encoding procedure using different parameters, in alternative embodiments of the invention, different code classes are generated by the same parameters and different encoding algorithms, or different encoding algorithms and different sets of parameters.

[0027] At block 211, a different encoding scheme is selected. The different encoding scheme is different in at least one aspect from the previously selected encoding scheme (e.g., different parameters, a different encoding algorithm, etc.).

[0028] At block 213, the next code class is generated by applying the selected encoding scheme to the encoded data processed at block 205. At block 215, it is determined if the encoding is complete. If the encoding is not complete, then control flows back to block 211. If the encoding is complete, then control flows to block 217.

[0029] At block 217, the encoded data is transmitted. The symbols of the data are encoded so that each symbol is a member of at least one code word of each code class.

[0030] While the flow diagrams in the Figures show a particular order of operations performed by certain embodiments of the invention, it should be understood that such order is exemplary (e.g., alternative embodiments of the invention may perform certain of the operations in a different order, combine certain of the operations, perform certain of the operations in parallel, etc.). For example, block 201 and/or block 211 may not be performed if the set of parameters are predetermined. In addition, block 203 may be performed before block 201. In another embodiment of the invention, block 201 and block 211 are performed sequentially or in parallel.

[0031] Encoding of symbols so that each symbol is a member of at least one code word of each code class may be illustrated with a matrix. Figures 3A – 3C are diagrams illustrating interleaving of code classes.

[0032] Figure 3A is a diagram illustrating exemplary interleaving of two code classes in a matrix according to one embodiment of the invention. In Figure 3A, wrapped data 301 is processed by an encoding procedure 305. The encoding procedure 305 generates a first code class illustrated as a set of k_2 code words arranged as rows in a matrix 309. Each code word of the first code class includes n_1 symbols of which k_1 symbols are information symbols to be protected. The redundancy symbols for the first code class are illustrated in the matrix 309 as row redundancy symbols 311 (n_1 - k_1 redundancy symbols for each row). The first code class corresponds to the first dimension of the matrix 309.

[0033] A second dimension of the matrix 309 is then processed by an encoding procedure 306. As previously stated, alternative embodiments of the invention may process the matrix 309 with another encoding procedure, with another encoding procedure and another set of parameters, etc. The encoding procedure 306 generates a matrix 315. The columns of the matrix 315 are the code words of the second code

class. The code words of the second code class have a block length of n_2, k_2 information symbols, and $n_2 - k_2$ redundancy symbols for each code word, which are illustrated as column redundancy symbols 313. The second code class includes n_1 code words (i.e., n_1 columns in the matrix 315). The second code class includes code words comprised of the row redundancy symbols 311 and redundancy symbols for correction of the row redundancy symbols 311.

[0034] Figure 3B is a diagram illustrating exemplary interleaving of a third code class into the matrix of Figure 3A according to one embodiment of the invention. In Figure 3B, an encoding procedure 316 generates a matrix 319. The encoding procedure 319 encodes a third dimension of the matrix 306 to generate the matrix 319 with a third code class. The matrix 319 includes third dimension redundancy symbols 317. The third dimension redundancy symbols 317 correspond to each diagonal of the code words of the third code class.

[0035] Figure 3C is a diagram illustrating an alternative exemplary interleaving of two code classes according to one embodiment of the invention. Figure 3C illustrates the encoding procedure 105 generating a stream of interleaved code classes as a two-dimensional field 321. Field 321 includes row code words and column code words. Unlike the matrix 315 of Figure 3A, the field 321 includes multiple code words in each row. In the field 321, the code words of the first code class do not align against a single code word of the second code class.

[0036] Interleaving multiple code classes provides for improved forward error correction. Each single FEC encoding scheme imposes hard restrictions on the transmission error distribution, like a fixed error limit per code word. Interleaving multiple code classes enables iterative decoding to widely overcome this limitation of

FEC encoding schemes, resulting in drastically improved performance, especially for Averaged White Gaussian Noise (AWGN) models.

[0037] Figure 4 is a flow chart for the decoding of data according to one embodiment of the invention. At block 401 data is received. At block 402, the last code class (i.e., the last code class that was encoded at a transmitting network element) is processed. At block 403, the next code class (i.e., the code class encoded prior to the last code class at the transmitting network element) is processed. At block 405, it is determined if all of the code classes have been decoded. If all of the code classes have not been decoded, then control flows back to block 403. If all of the code classes have been decoded, then control flows to block 407.

[0038] At block 407 it is determined if any errors were corrected while processing all code classes. If any errors were corrected, then control flows from block 407 back to block 402. If no further errors were corrected, then at block 409 the redundancy symbols are removed from the received data.

[0039] Figure 4 illustrates how interleaving multiple code classes enables iterative decoding to overcome the limitations of current FEC encoding schemes. For example, assume the encoding procedures 305 and 306 individually provide for correction of t_1 and t_2 transmission errors, respectively. If the number of errors in a code word of the first code class exceed t_1, then that code word typically could not be corrected. Since multiple code classes are interleaved and then iteratively decoded, corrected errors in the second code class possibly enable corrections in the first code class in a subsequent iteration. In other words, correction of an incorrect symbol that is at an intersection of code words of the first and second code class may reduce the number of errors in code word of the first code class below t_1. Thus this code word becomes correctable in the next iteration round.

[0040] As previously indicated, the order of operations illustrated in Figure 4 is exemplary. For example, block 405 may not be performed because the number of code classes is known. Alternative embodiments of the invention may perform block 407 differently. Instead of observing performed error correction a fixed number of iterative cycles may be given. In addition, another embodiment of the invention may accept a certain level of error remaining in the outgoing data. In another embodiment of the invention, processing the single code classes (blocks 402 and 403) may be performed in parallel in the form of a pipelined architecture as illustrated in Figure 5.

[0041] Figure 5 is a diagram of components of a line card of a network element according to one embodiment of the invention. In Figure 5, a line card 500 includes an optical receiver 501 receives wrapped data as an optical signal. The optical receiver 501 converts an optical signal into an electrical signal. The optical receiver 501 then passes wrapped data in electrical signal form to a deserializer 503. The deserializer 503 arranges the wrapped data for iterative decoding. The deserializer 503 then passes the wrapped data to be processed by a series of arbitrary number of iterative decoders 505A - 505F. Each of the iterative decoders 505A - 505F performs at least one iteration of decoding on all code classes of the wrapped data. The iterative decoder 505F passes the wrapped data to an iterative decoder/dewrapper and encoder/wrapper 509. The iterative decoder/dewrapper and encoder/wrapper 509 performs at least one more iteration of decoding all of the code classes of the data and dewraps the data. The iterative decoder/dewrapper and encoder/wrapper 509 then outputs the data.

[0042] The iterative decoder/dewrapper and encoder/wrapper 509 also receives data to be transmitted. The iterative decoder/dewrapper and encoder/wrapper 509 wraps the received data as described in Figure 1A and encodes the received data as previously described in Figures 1-2. The iterative decoder/dewrapper and encoder/wrapper 509

then passes the wrapped and encoded data to a serializer 511. The serializer 511 arranges the wrapped data for transmission. The serializer 511 then passes the serialized wrapped data to an optical transmitter 513. The optical transmitter 513 converts the serialized wrapped data from an electrical signal to an optical signal and transmits the optical signal.

[0043] The line card 500 and/or the components of the line card 500 include one or more machine-readable media. A machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical, acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.); etc.

[0044] The embodiment of the invention illustrated in Figure 5 is scalable by the number of iterative decoders coupled together. In addition, the illustrated embodiment of the invention provides substantial board space savings by implementing the encoder and the decoder as a single component. Various embodiments of the invention may implement the iterative decoders differently. For example, the iterative decoders 505A – 505F may be implemented as a single iterative FEC decoder, the iterative decoders 505A – 505F and the decoding function in the iterative decoder/dewrapper and encoder/wrapper unit 509 may be implemented as a single unit.

[0045] Figure 6A is a diagram illustrating an exemplary embodiment of the invention of the iterative decoder 505A of Figure 5 according to one embodiment of the invention. In Figure 6A, the iterative decoder 505A is for decoding two code classes. In Figure 6A, a column decoder 601 of the iterative decoder 505A receives wrapped data. The column decoder 601 decodes each column of the received data. After

decoding each column of the received data, the column decoder 601 passes the data to a data reorderer 603A. The data reorderer 603A rearranges the data received from the column decoder 601 from a column perspective to a row perspective. The data reorderer 603A then passes the reordered data to a row decoder 605. The row decoder 605 decodes the received data as rows of a matrix. The row decoder 605 then passes the data to a data reorderer 603B. The data reorderer 603B rearranges the data from the perspective of rows to columns. The data reorderer 603B then passes the reordered data to the next iterative decoder.

[0046] Figure 6B is a diagram illustrating an exemplary embodiment of the invention of the iterative decoder/dewrapper and encoder/wrapper 509 according to one embodiment of the invention. In Figure 6B, the iterative decoder 505F passes data to the iterative decoder/dewrapper and encoder/wrapper ("hybrid unit") 509. The data passes through the column decoder 601A, data reorderer 603A, and a row decoder 605A, similar to each of the iterative decoders 505A-505F. The row decoder 605A passes the data to the dewrapper 611. The dewrapper 611 dewraps the data similar to the dewrapping previously described in Figure 1. The hybrid unit 509 also includes a wrapper 613. The wrapper 613 receives data to be transmitted and wraps the data similar to the wrapping previously described with respect to Figure 1. The wrapper 613 passes the wrapped data to a row encoder 615. The row encoder 615 fills in some of the space added by the wrapper 613 with row redundancy symbols. The row encoder 615 then passes this data to a data reorderer 603B. The data reorderer 603B reorders the data from a row perspective to a column perspective. The data reorderer 603B then passes the reordered data to a column encoder 607. The column encoder 607 fills the rest of the space added by the wrapper 613 with column redundancy symbols. The

column encoder 607 then passes the data out of the iterative decoder/dewrapper and encoder/wrapper 509.

[0047] Figure 7 is a diagram illustrating an iterative decoder with backward annotation according to one embodiment of the invention. The iterative decoder illustrated in Figure 7 is an exemplary three code class iterative decoder. For simplicity it is assumed, that each code class is of algebraic nature comprising the computation for syndromes as a first step. An iterative decoder 700 illustrated in Figure 7 includes syndrome computation units 703A - 703C. Alternative embodiments of the invention may include more or less syndrome computation units. Error pattern computation units 709A – 709C are coupled with the syndrome computation units 703A – 703C. The iterative decoder 700 receives data having three code classes. The received data is stored in a FIFO 701A. The received data is also sent to the syndrome computation units 703A – 703C.

[0048] The syndrome computation unit 703A computes the syndrome for the third code class. The syndrome computation unit 703A passes the syndrome to an error pattern computation unit 709A. The error pattern computation unit 709A calculates error patterns for error correction and also calculates a back annotation. The corrections determined by the error pattern computation unit 709A are applied to the data stored in the FIFO 701A. The resulting data is stored in a FIFO 701B. The calculated back annotation is passed from the error pattern computation unit 709A to the syndrome computation units 703B and 703C. Since syndrome computation is linear, the syndrome computation units 703A – 703C compute their syndromes in parallel, hence the syndrome computation unit 703B has calculated a syndrome for the second code class. The syndrome computation unit 703B adds the received back annotation to its computed syndrome. The syndrome computation unit 703B then

passes the syndrome with back annotation to the error pattern computation unit 709B. The error pattern computation unit 709B performs the same task as the error pattern computation unit 709A for the second code class.

[0049] The error pattern computation unit 709B applies the computed error correction information to the data stored in the FIFO 701B. The resulting data is stored in a FIFO 701C. The error pattern computation 709B passes the back annotation computed for the second code class to the syndrome computation unit 703C. The syndrome computation unit 703C should have computed a syndrome for the first code class and added the first code classes back annotation. The syndrome computation unit 703C then adds the back annotation for the second code class to its syndrome and passes the computed syndrome to the error pattern computation unit 709C. The error pattern computation unit 709C determines error correction information and applies the information to the data stored in the FIFO 701C. The resulting data is then passed to the next iterative decoder.

[0050] Iterative decoding of interleaved code classes with backward annotation reduces latency from decoding each code class. The error patterns of a code class C_1 may be computed immediately after error pattern computation of a code class C_2 has completed.

[0051] Figure 8 is a diagram illustrating an iterative decoder with forward annotation according to one embodiment of the invention. An iterative decoder 800 illustrated in Figure 8 is similar to the iterative decoder 700 illustrated in Figure 7. The iterative decoder 800 includes syndrome computation units 803A - 803C. Alternative embodiments of the invention may include more or less syndrome computation units. Error pattern computation units 809A – 809C are coupled with the syndrome computation units 803A – 803C. The iterative decoder 800 receives data having three

code classes. The received data is stored in a FIFO 801A. The received data is also sent to the syndrome computation units 803A – 803C.

[0052] The syndrome computation unit 803A computes the syndrome for the third code class. The syndrome computation unit 803A passes the syndrome to an error pattern computation unit 809A. The error pattern computation unit 809A calculates error patterns for error correction and also calculates a back annotation. The corrections determined by the error pattern computation unit 809A are applied to the data stored in the FIFO 801A. The resulting data is stored in a FIFO 801B. The calculated back annotation is passed from the error pattern computation unit 809A to the syndrome computation units 803B and 803C. Since syndrome computation is linear, the syndrome computation units 803A – 803C compute their syndromes in parallel, hence the syndrome computation unit 803B has calculated a syndrome for the second code class. The error pattern computation unit 809A also stored its computed results in a buffer 811 for transmission to a syndrome computation unit of the next iterative decoder ("forward annotation"). The syndrome computation unit 803B adds the received back annotation to its computed syndrome. The syndrome computation unit 803B then passes the syndrome with back annotation to the error pattern computation unit 809B. The error pattern computation unit 809B performs the same task as the error pattern computation unit 809A for the second code class.

[0053] The error pattern computation unit 809B applies the computed error correction information to the data stored in the FIFO 801B. The resulting data is stored in a FIFO 801C. The error pattern computation 809B passes the back annotation computed for the second code class to the syndrome computation unit 803C and stores the computed error pattern in the buffer 811 for transmission to a syndrome computation unit of the next iterative decoder. The syndrome computation unit 803C

should have computed a syndrome for the first code class and added the first code classes back annotation. The syndrome computation unit 803C then adds the back annotation for the second code class to its syndrome and passes the computed syndrome to the error pattern computation unit 809C. The error pattern computation unit 809C determines error correction information and applies the information to the data stored in the FIFO 801C. As with the error pattern computation units 809A – 809B, the error pattern computation unit 809C passes its computed error pattern to the buffer 811 for transmission to a syndrome computation unit of the next iterative decoder. The data stored in the FIFO 801C passed to the next iterative decoder.

[0054] In one embodiment of the invention, the buffer 811 temporarily hosts computed annotations to be transmitted to the syndrome computation units of the next iterative decoder as indicated by the error pattern computation units. In alternative embodiments of the invention, error pattern computation units pass forward annotation information to a buffer specifically corresponding to the error pattern computation unit of an iterative decoder and a syndrome computation unit of the next iterative decoder. In another embodiment of the invention, error pattern computation units of an iterative decoder pass computed error patterns directly its corresponding syndrome computation unit of the next iterative decoder. Forward annotation reduces latency.

[0055] The described iterative decoding may be implemented by instructions stored on one or more machine-readable media. Thus, a machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g., a computer). For example, a machine-readable medium includes read only memory (ROM); random access memory (RAM); magnetic disk storage media; optical storage media; flash memory devices; electrical, optical,

acoustical or other form of propagated signals (e.g., carrier waves, infrared signals, digital signals, etc.), etc.

[0056] As previously described, iterative hard decision decoding of interleaved code classes enables forward error correction for optical transmissions.

[0057] While the invention has been described in terms of several embodiments of the invention, those skilled in the art will recognize that the invention is not limited to the embodiments of the invention described. The method and apparatus of the invention may be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting on the invention. .

CLAIMS

What is claimed is:

1. An apparatus comprising:

a binary receiver to convert an optical signal to an electrical signal, the electrical signal having a set of information symbols and a set of redundancy symbols, the set of redundancy symbols generated by different forward error correction (FEC) encoding schemes; and

a first of a plurality of decoders coupled with the binary receiver and the plurality of decoders coupled together, each of the plurality of decoders to decode the set of information symbols with the set of redundancy symbols in accordance with the different FEC encoding schemes.

2. The apparatus of claim 1 wherein the plurality of decoders are coupled together serially.

3. The apparatus of claim 1 wherein the different FEC encoding schemes are the same FEC encoding algorithm with different parameters.

4. The apparatus of claim 1 wherein the different FEC encoding schemes are different FEC encoding algorithms.

5. The apparatus of claim 1 further comprising a deserializer coupled with the binary receiver to de-serialize the electrical signal.

6. The apparatus of claim 1 further comprising a decoder/de-wrapper coupled with one of the plurality of decoders, the unit to decode the set of information symbols with the set of redundancy symbols in accordance with the different FEC encoding schemes and to remove the set of redundancy symbols.

7. The apparatus of claim 1 further comprising a de-wrapper coupled with one of the plurality of decoders, the de-wrapper to remove the set of redundancy symbols.

8. The apparatus of claim 1 further comprising a decoder/de-wrapper/encoder/wrapper unit coupled with one of the plurality of decoders, the decoder/de-wrapper/encoder/wrapper unit to decode the set of information symbols with the set of redundancy symbols in accordance with the different FEC encoding schemes, to remove the set of redundancy symbols, to receive a second set of information symbols, to add overhead space and overhead information to the set of redundancy symbols, and to encode the set of information symbols with the different FEC encoding schemes.

9. The apparatus of claim 8 further comprising a binary transmitter coupled with the decoder/de-wrapper/encoder/wrapper unit, the binary transmitter to convert an electrical signal received from the decoder/de-wrapper/encoder/wrapper unit to an optical signal.

10. The apparatus of claim 8 further comprising a serializer coupled with the decoder/de-wrapper/encoder/wrapper unit, the serializer to serialize an electrical signal received from the decoder/de-wrapper/encoder/wrapper unit.

11. An apparatus comprising:

a binary receiver to receive an optical signal and to convert the optical signal to an electrical signal;

an iterative forward error correction (FEC) decoder coupled with the binary receiver, the iterative FEC decoder to repeatedly decode each code class of a set of data having multiple interleaved code classes a given number of times; and

a dewrapper coupled with the iterative FEC decoder, the dewrapper to remove redundancy symbols and overheard information from the set of data.

12. The apparatus of claim 11 further comprising a wrapper coupled with the dewrapper to add overhead space and overhead information to data to be transmitted from the apparatus.

13. The apparatus of claim 12 further comprising a serializer coupled with the dewrapper.

14. The apparatus of claim 13 further comprising a transmitter coupled with the serializer.

15. The apparatus of claim 11 further comprising an encoder coupled with the dewrapper, the encoder to encode data to be transmitted from the apparatus.

16. An apparatus comprising:

a first decoder having

a plurality of forward error correction (FEC) encoding scheme decoders alternatingly coupled with a plurality of data reorderers, each of the plurality of FEC encoding scheme decoders to decode data in accordance with different FEC encoding schemes and each of the plurality of data reorderers to arrange the data for a subsequent one of the plurality of FEC encoding scheme decoders; and

a second decoder coupled with the first decoder.

17. The apparatus of claim 16 further comprising a de-wrapper coupled with the second decoder, the de-wrapper to remove redundancy symbols from the data.

18. The apparatus of claim 16 wherein each of the plurality data reorderers arranges the data in accordance with a corresponding dimension.

19. The apparatus of claim 16 further comprising a binary receiver coupled with the first decoder, the binary receiver to convert a signal from optical to electrical, the signal having the set of information symbols and the first and second set of redundancy symbols.

20. An apparatus comprising:

a first decoder having

a first buffer to receive a set of data, the set of data including a set of code words,

a first syndrome computation unit to receive the set of data and to compute a first syndrome for the set of data in accordance with a first forward error correction (FEC) encoding scheme,

a first error pattern computation unit coupled with the first syndrome computation unit, the first error pattern computation unit to compute a first error pattern with the first syndrome, to update the set of data in the first buffer, and to compute a first value,

a second buffer coupled with the first buffer, the second buffer to receive the updated set of data,

a second syndrome computation unit coupled with the first error pattern computation unit, the second syndrome computation unit to receive the set of data and to compute a second syndrome for the set of data in accordance with a second FEC encoding scheme, to receive the first value and to update the second syndrome with the first value,

a second error pattern computation unit coupled with the second syndrome computation unit and the second buffer, the second

error pattern computation unit to compute a second error pattern and to update the set of data in the second buffer; and

a second decoder coupled with the first decoder, the second decoder to receive the set of data from the first decoder.

21. The apparatus of claim 20 further comprising a binary receiver coupled with the first decoder, the binary receiver to convert a signal from optical to electrical, the signal having the set of data.

22. The apparatus of claim 20 further comprising a de-wrapper coupled with the second decoder, the de-wrapper to remove redundancy symbols from the set of data.

23. The apparatus of claim 20 further comprising:

the first decoder further having

the second error pattern computation unit to compute a second value,

a third buffer to receive the updated set of data from the second buffer,

a third syndrome computation unit coupled with the first and second error pattern computation units, the third syndrome computation unit to compute a third syndrome and to update the syndrome with the second value, and

a third error pattern computation unit coupled with the third syndrome computation unit, the third error pattern computation unit to compute a third error patter for the set of data and to update the set of data in the third buffer.

24. The apparatus of claim 20 further comprising a third buffer coupled with the first and second error pattern computation units and a third and fourth syndrome computation units of the second decoder, the third buffer to receive the first value and

the second value and to send the first value to the third syndrome computation unit and to send the second value to the fourth syndrome computation unit.

25. The apparatus of claim 20 further comprising:

the second decoder having

a third syndrome computation unit coupled with the first and the second error pattern computation units of the first decoder, the third syndrome computation unit to receive the first value and the second value, and

a fourth syndrome computation unit coupled with the first and second error computation units of the first decoder, the fourth syndrome computation unit to receive the first and second value.

26. An apparatus comprising:

a binary receiver to receive a signal and to convert the signal from optical to electrical, the signal having a set of data;

a first decoder coupled with the binary receiver, the first decoder to decode the set of data in accordance with a plurality of different forward error correction (FEC) encoding schemes;

a second decoder coupled with the first decoder, the second decoder to decode the set of data in accordance with the plurality of different FEC encoding schemes;

a de-wrapper coupled with the second decoder, the de-wrapper to remove redundancy symbols from the set of data;

a wrapper to receive a second signal, the second signal having a second set of data, the wrapper to add overhead space and overhead information to the second set of data;

an encoder coupled with the wrapper, the encoder to encode the second set of data with the plurality of different FEC encoding schemes; and

a binary transmitter coupled with the encoder, the binary transmitter to convert the second signal from electrical to optical.

27. The apparatus of claim 26 wherein the first and second decoder each comprise a plurality of FEC encoding scheme decoders alternatingly coupled with a plurality of data reorderers, the each of the FEC encoding scheme decoders to decode the set of data in accordance with a different one of the plurality of different FEC encoding schemes and the plurality of data reorderers to arrange the set of data.

28. The apparatus of claim 26 wherein the first and second decoder each comprise:

a first buffer;

a first syndrome computation unit;

a first error pattern computation unit coupled with the first syndrome computation unit and the first buffer;

a second buffer coupled with the first buffer;

a second syndrome computation unit coupled with the first error pattern computation unit; and

a second error pattern computation unit coupled with the second syndrome computation unit and the second buffer.

29. The apparatus of claim 28 wherein the first and second error pattern computation units of the first decoder are coupled with the first and second syndrome computation units of the second decoder.

30. The apparatus of claim 28 wherein the first and second error pattern computation units are coupled with a third buffer that is coupled with the first and second syndrome computation units of the second decoder.

31. The apparatus of claim 26 further comprising a serializer coupled with the binary transmitter and the encoder, the serializer to serialize the second set of data.

32. The apparatus of claim 26 further comprising a deserializer coupled with the binary receiver and the first decoder, the deserializer to deserialize the set of data.

33. A system comprising:

a first network element having

a wrapper to add overhead space and overhead information to a set of data,

an encoder coupled with the wrapper, the encoder to encode the set of data in accordance with a plurality of different forward error correction (FEC) schemes,

a binary transmitter coupled with the encoder, the binary transmitter to convert the set of data from an electrical signal to an optical signal; and

a second network element coupled with the first network element, the second network element having

a binary receiver to convert the set of data from the optical signal to the electrical signal,

a first decoder coupled with the binary receiver, the first decoder to decode the set of data in accordance with the plurality of different FEC encoding schemes,

a second decoder coupled with the first decoder, the second decoder to decode the set of data in accordance with the plurality of different FEC encoding schemes; and

a de-wrapper coupled with the second decoder, the de-wrapper to remove overhead space, overhead information, and redundancy symbols from the set of data.

34. The system of claim 33 further comprising:

the first network element having

a third decoder to decode a second set of data in accordance with the plurality of different FEC encoding schemes, and

a fourth decoder coupled with the third decoder, the fourth decoder to decode the second set of data in accordance with the plurality of different FEC encoding schemes.

35. The system of claim 33 further comprising:

the second network element having

a second wrapper to add overhead space and overhead information to a second set of data,

a second encoder coupled with the second wrapper, the second encoder to encode the second set of data in accordance with the plurality of different forward error correction (FEC) schemes, and

a second binary transmitter coupled with the second encoder, the second binary transmitter to convert the second set of data from a second electrical signal to a second optical signal

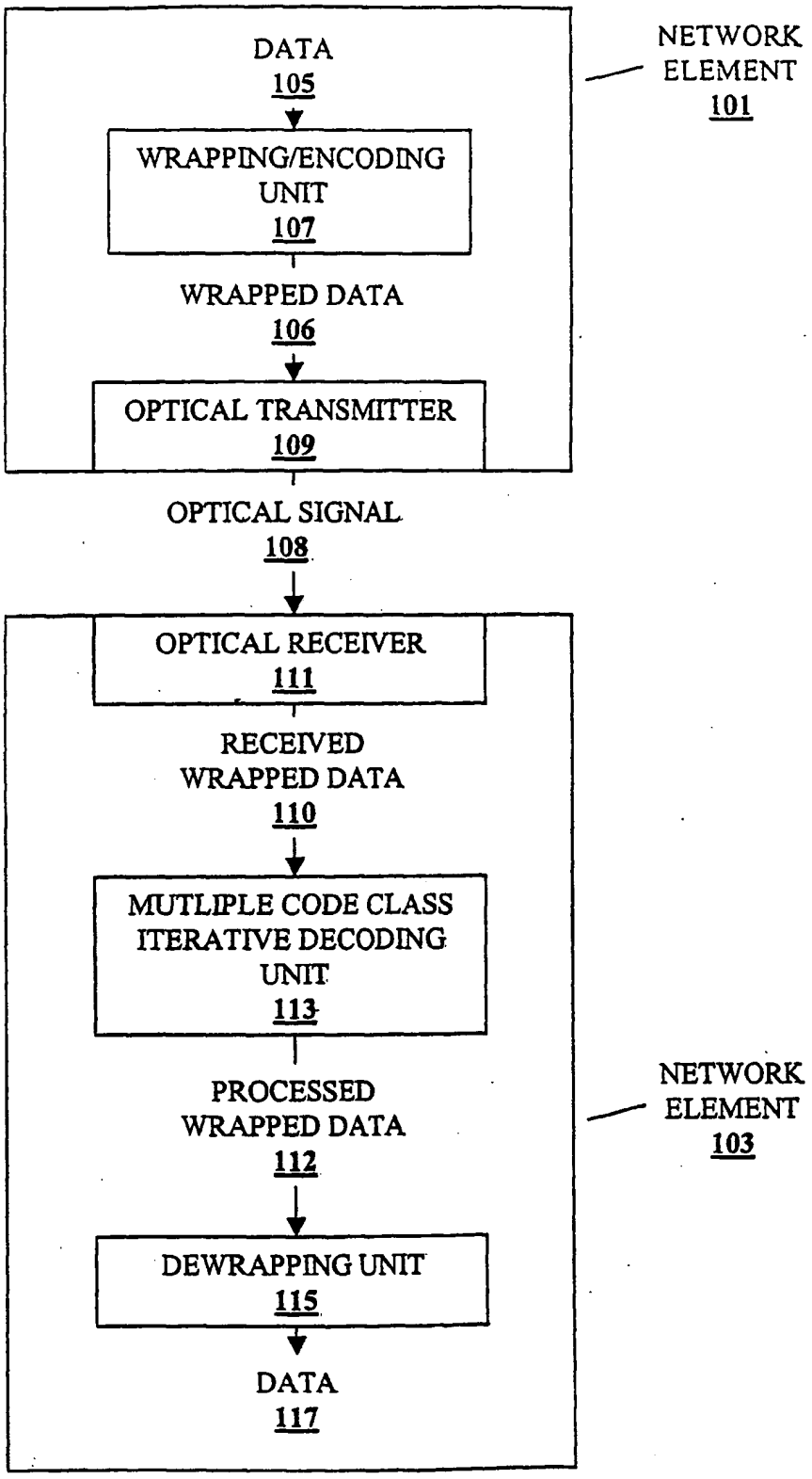
DATA
105
WRAPPING/ENCODING UNIT
107
WRAPPED DATA
106
OPTICAL TRANSMITTER
109
NETWORK ELEMENT
101
OPTICAL SIGNAL
108
OPTICAL RECEIVER
111
RECEIVED WRAPPED DATA
110
MUTLIPLE CODE CLASS ITERATIVE DECODING UNIT
113
PROCESSED WRAPPED DATA
112
DEWRAPPING UNIT
115
DATA
117
NETWORK ELEMENT
103

FIG. 1A

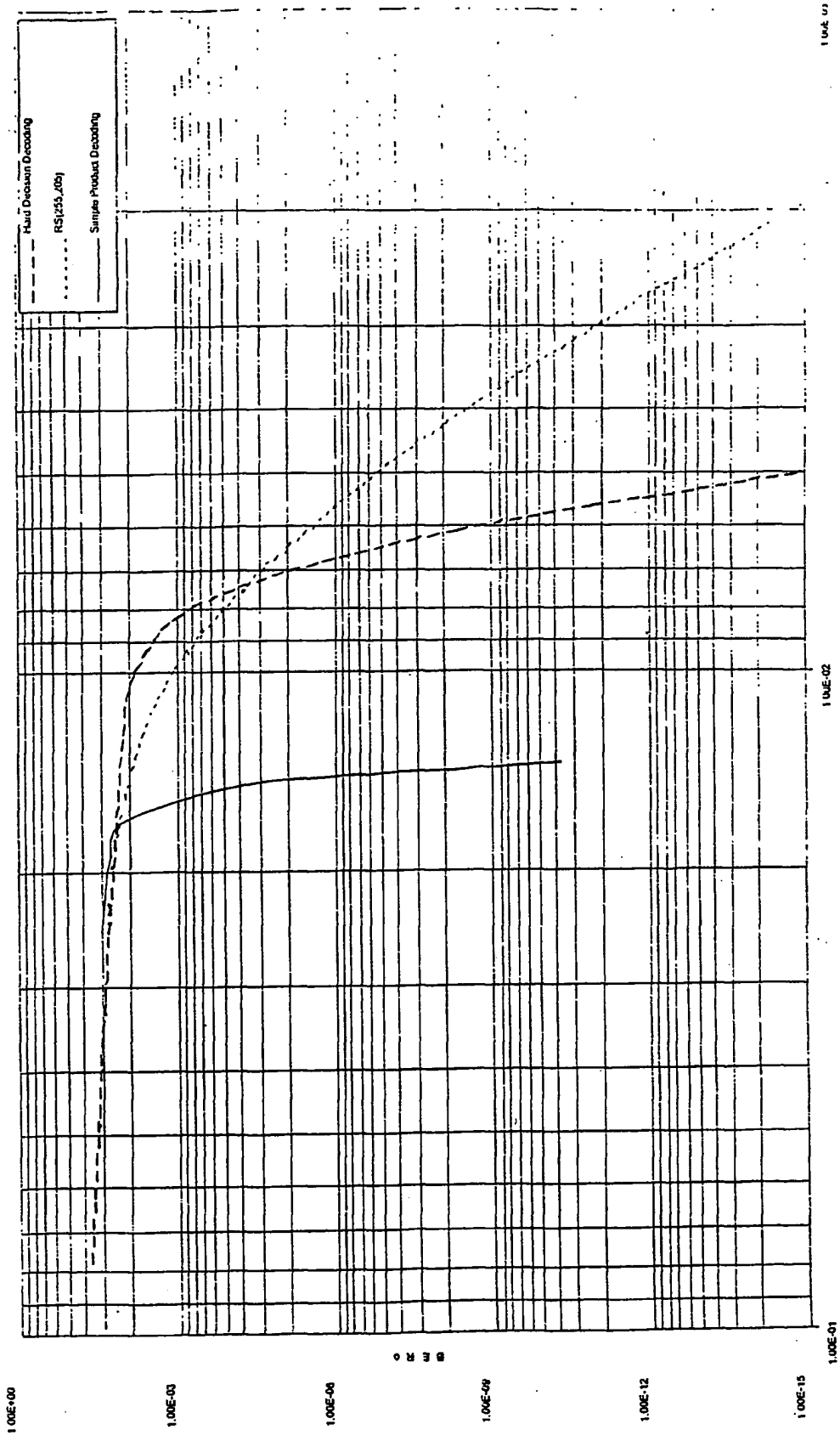
Hard Decision Decoding
RS(255,205)
Sample Product Decoding
BER
1.00E+00
1.00E-03
1.00E-06
1.00E-09
1.00E-12
1.00E-15
1.00E-01
1.00E-02
BER

FIG. 1B

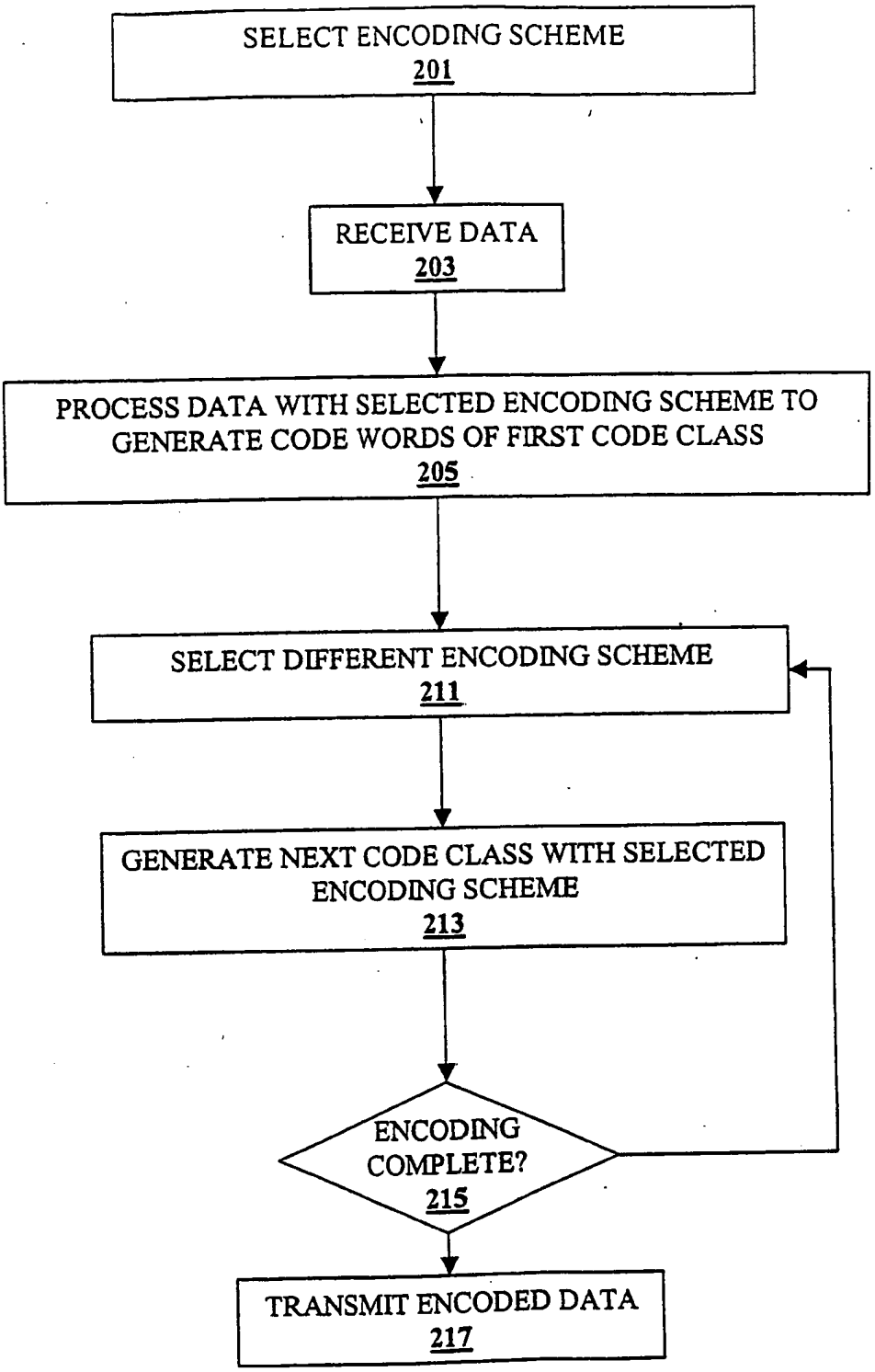
SELECT ENCODING SCHEME
201
RECEIVE DATA
203
PROCESS DATA WITH SELECTED ENCODING SCHEME TO GENERATE CODE WORDS OF FIRST CODE CLASS
205
SELECT DIFFERENT ENCODING SCHEME
211
GENERATE NEXT CODE CLASS WITH SELECTED ENCODING SCHEME
213
ENCODING COMPLETE?
215
TRANSMIT ENCODED DATA
217

FIG. 2

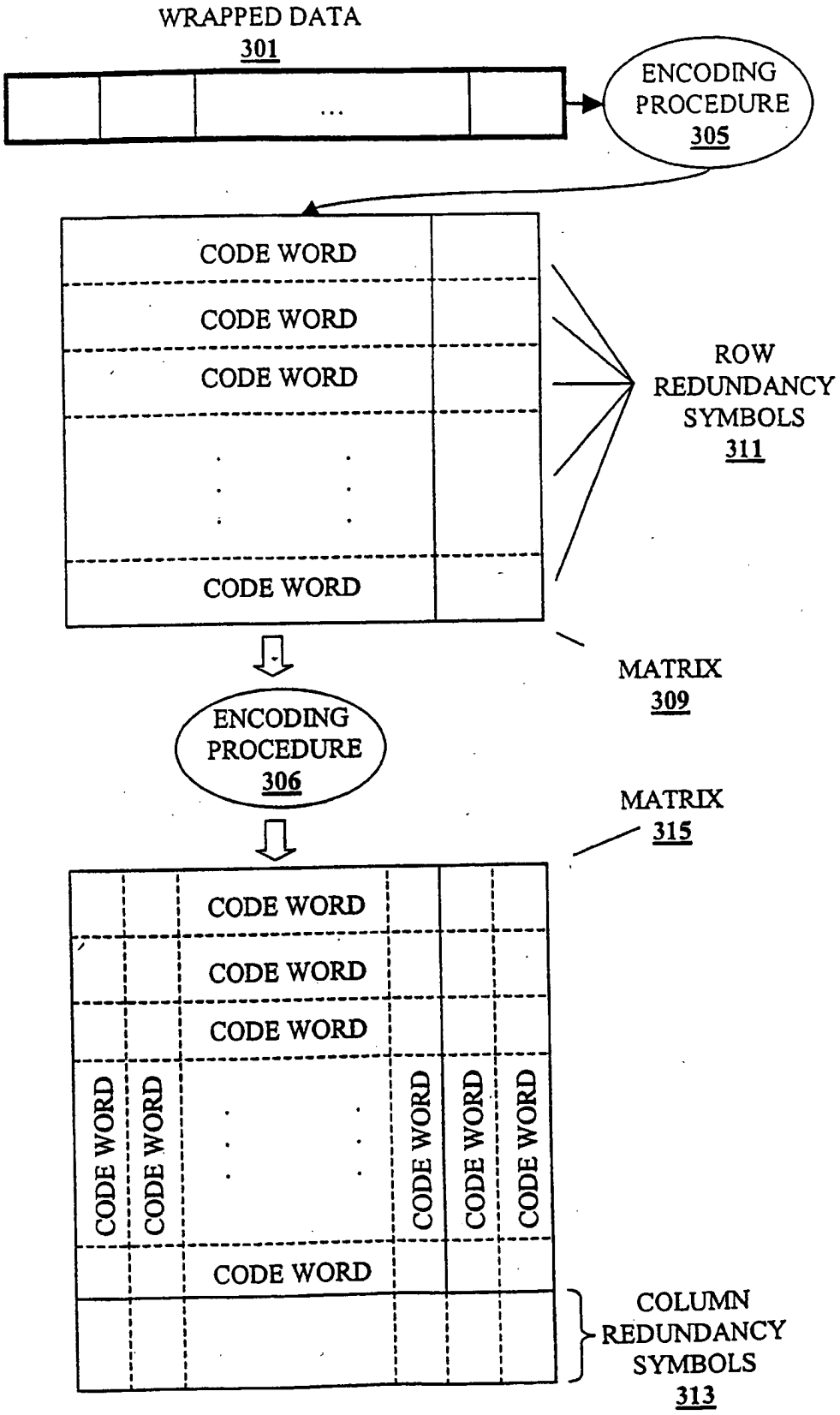
WRAPPED DATA
301
...
ENCODING PROCEDURE
305
CODE WORD
CODE WORD
CODE WORD
CODE WORD
ROW REDUNDANCY SYMBOLS
311
MATRIX
309
ENCODING PROCEDURE
306
MATRIX
315
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
COLUMN REDUNDANCY SYMBOLS
313

FIG. 3A

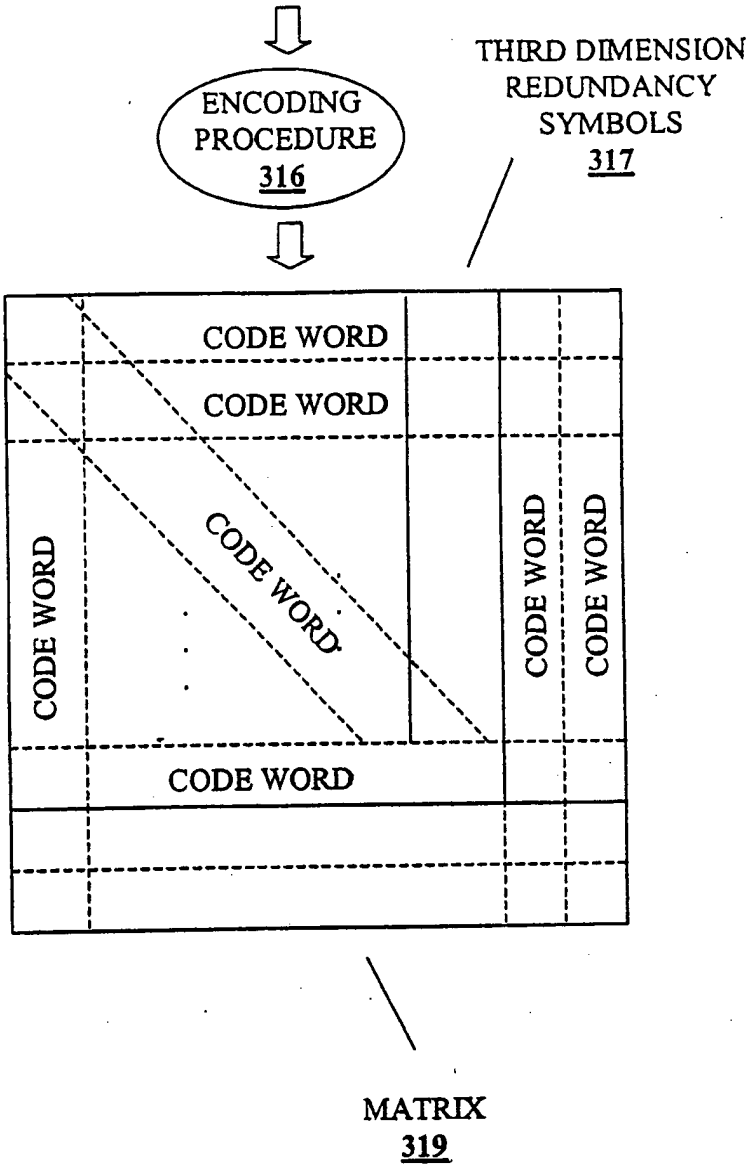
ENCODING PROCEDURE 316
THIRD DIMENSION REDUNDANCY SYMBOLS 317
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
MATRIX 319

FIG. 3B

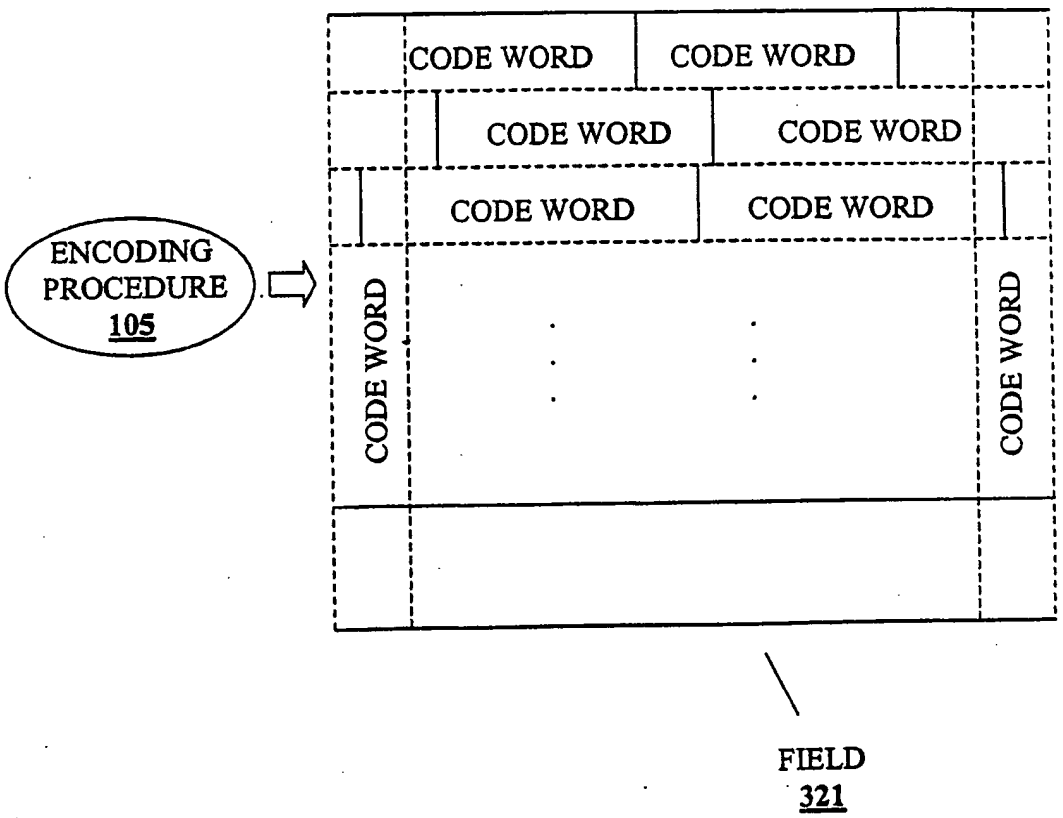
ENCODING PROCEDURE 105
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
CODE WORD
FIELD 321

FIG. 3C

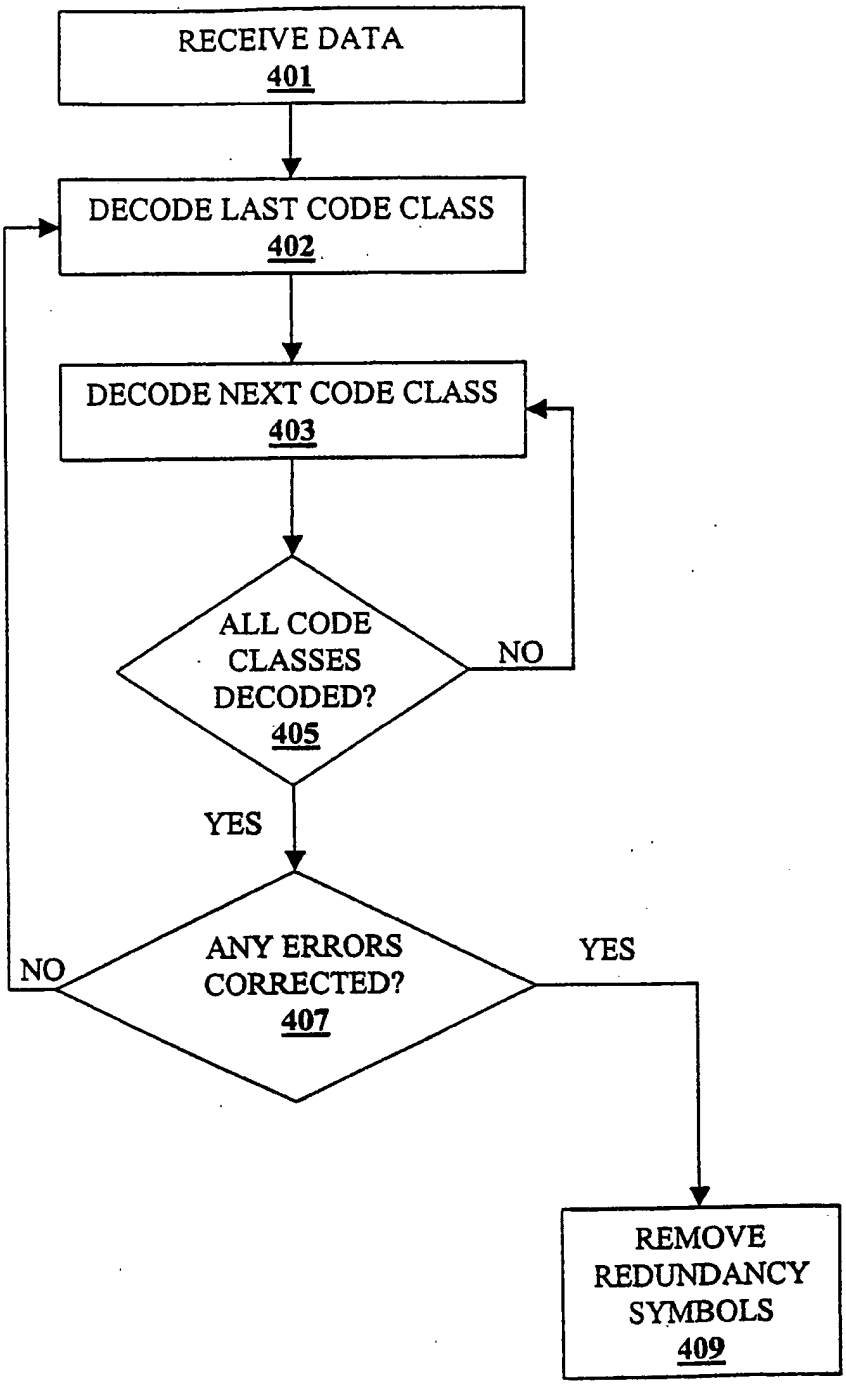
RECEIVE DATA
401
DECODE LAST CODE CLASS
402
DECODE NEXT CODE CLASS
403
ALL CODE CLASSES DECODED?
405
NO
YES
ANY ERRORS CORRECTED?
407
NO
YES
REMOVE REDUNDANCY SYMBOLS
409

FIG. 4

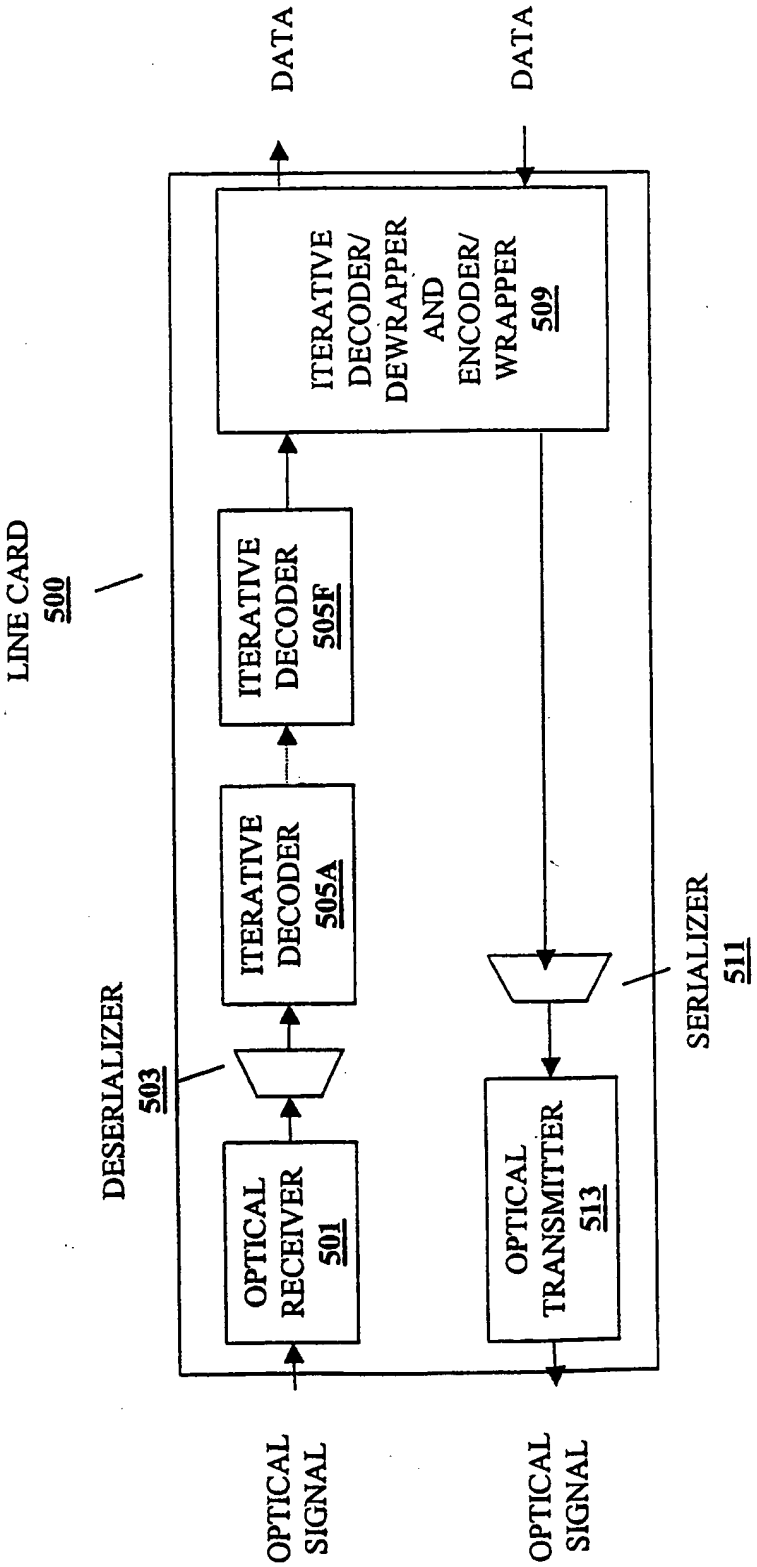
DATA
DATA
LINE CARD
500
ITERATIVE DECODER/ DEWRAPPER AND ENCODER/ WRAPPER
509
ITERATIVE DECODER
505F
ITERATIVE DECODER
505A
DESERIALIZER
503
SERIALIZER
511
OPTICAL RECEIVER
501
OPTICAL TRANSMITTER
513
OPTICAL SIGNAL
OPTICAL SIGNAL

FIG. 5

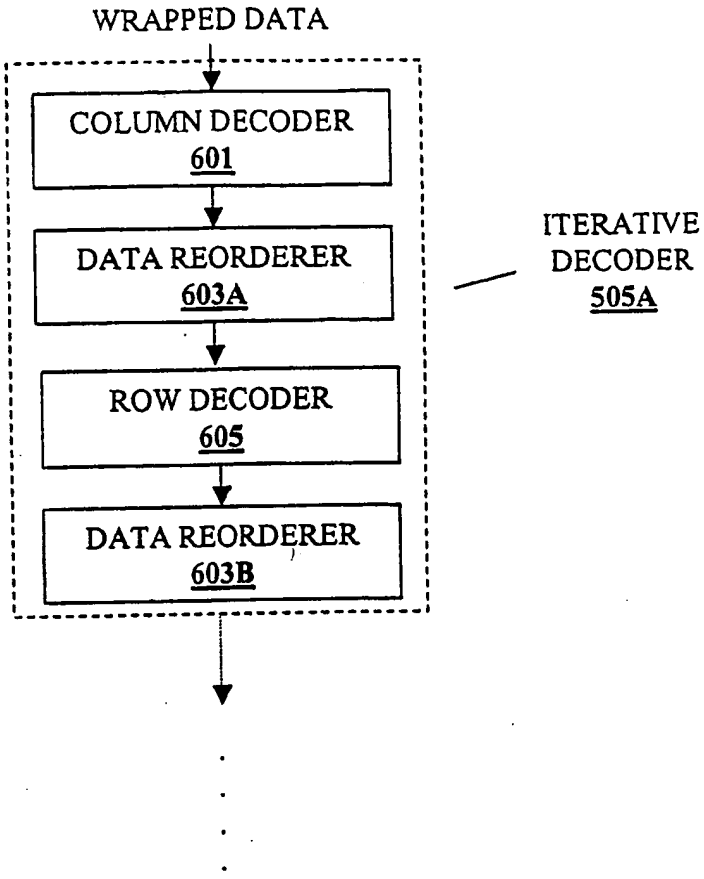
WRAPPED DATA
COLUMN DECODER
601
DATA REORDERER
603A
ROW DECODER
605
DATA REORDERER
603B
ITERATIVE
DECODER
505A

FIG. 6A

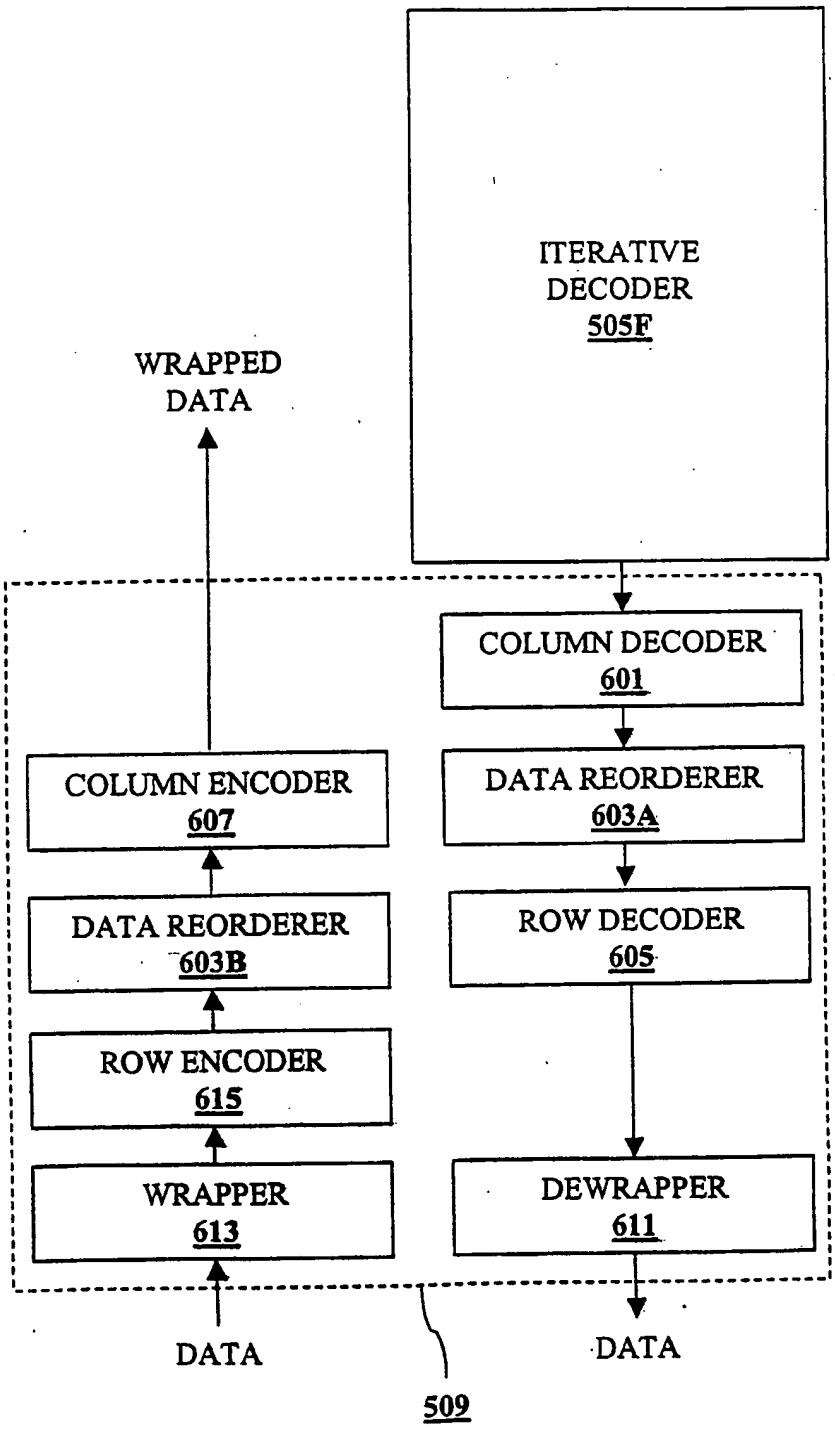
ITERATIVE DECODER 505F
WRAPPED DATA
COLUMN DECODER 601
COLUMN ENCODER 607
DATA REORDERER 603A
DATA REORDERER 603B
ROW DECODER 605
ROW ENCODER 615
WRAPPER 613
DEWRAPPER 611
DATA
DATA
509

FIG. 6B

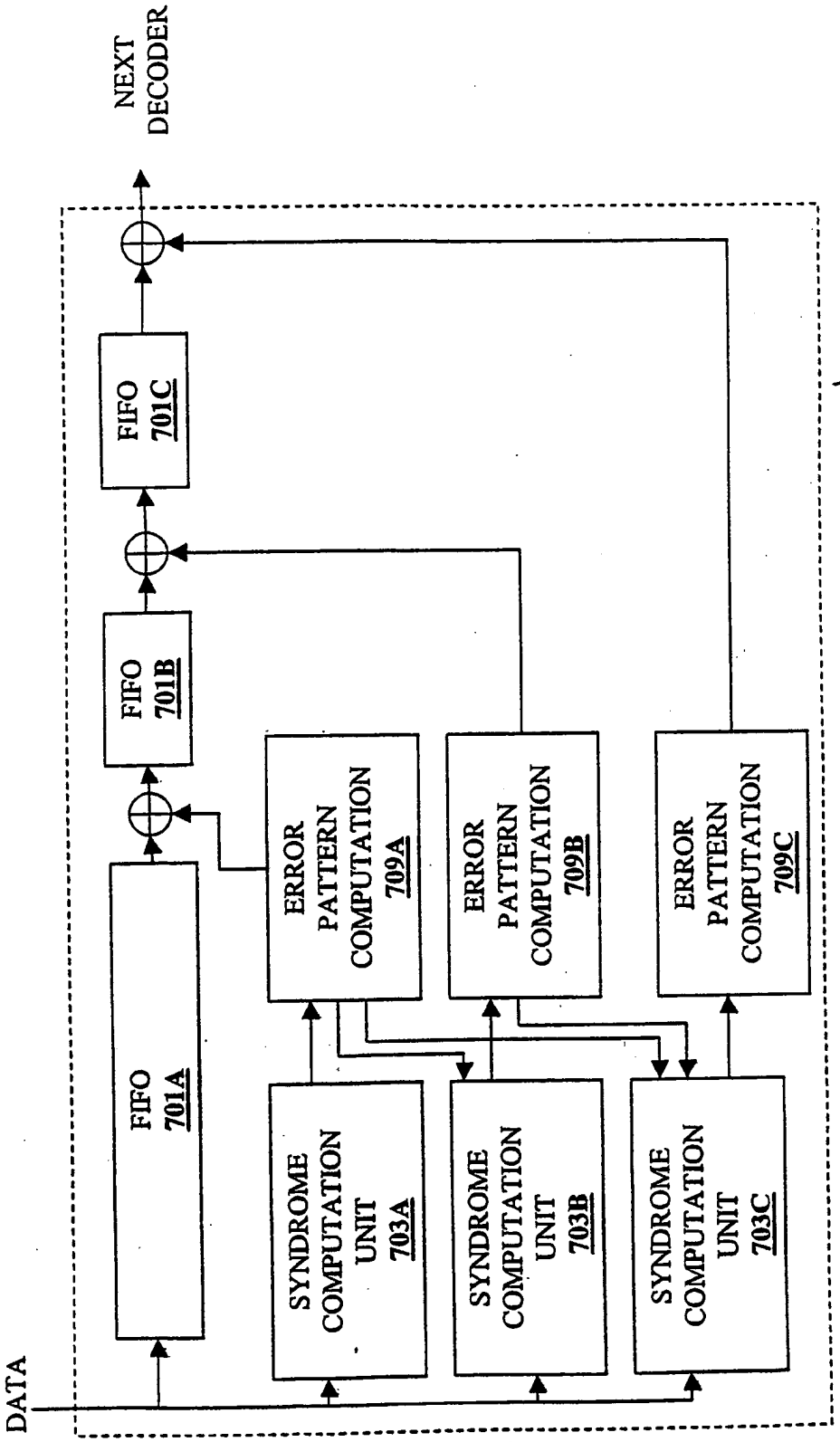
NEXT DECODER
FIFO 701C
FIFO 701B
FIFO 701A
ERROR PATTERN COMPUTATION 709A
ERROR PATTERN COMPUTATION 709B
ERROR PATTERN COMPUTATION 709C
SYNDROME COMPUTATION UNIT 703A
SYNDROME COMPUTATION UNIT 703B
SYNDROME COMPUTATION UNIT 703C
DATA
ITERATIVE DECODER 700

FIG. 7

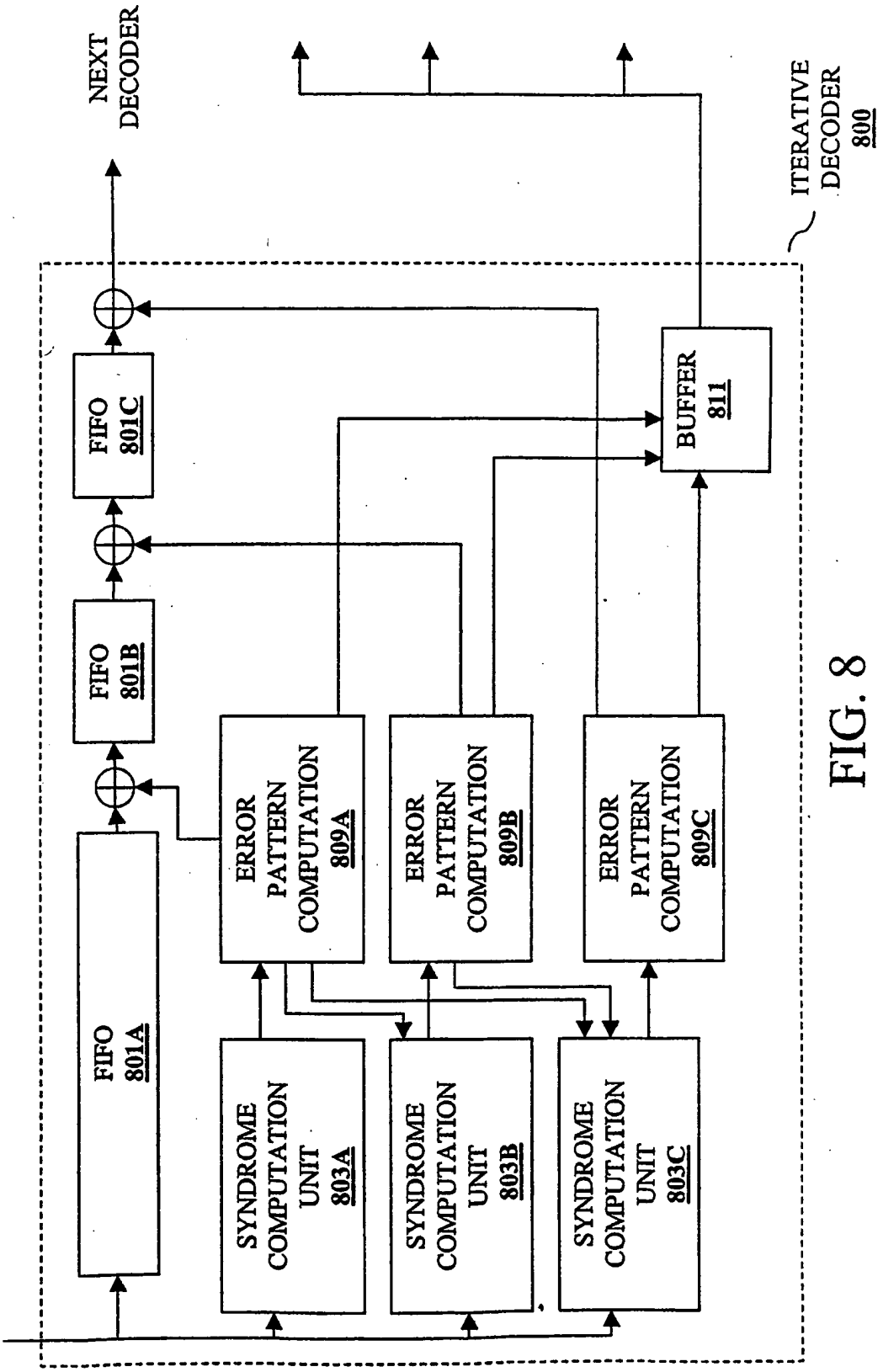
NEXT DECODER
ITERATIVE DECODER 800
FIFO 801C
FIFO 801B
FIFO 801A
BUFFER 811
ERROR PATTERN COMPUTATION 809A
ERROR PATTERN COMPUTATION 809B
ERROR PATTERN COMPUTATION 809C
SYNDROME COMPUTATION UNIT 803A
SYNDROME COMPUTATION UNIT 803B
SYNDROME COMPUTATION UNIT 803C

FIG. 8

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(74) Agents: **MALLIE, Michael, J.** et al.; Blakely, Sokoloff, Taylor & Zafman, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, CA 90025 (US).

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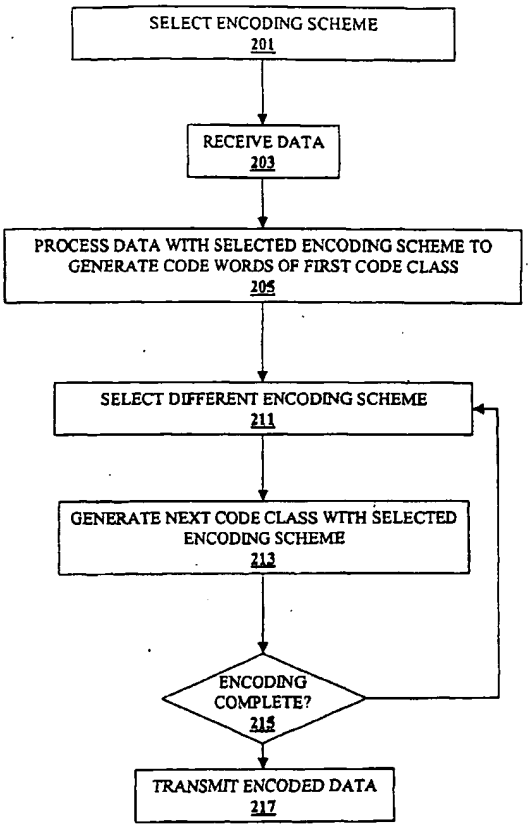
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: APPARATUS FOR ITERATIVE HARD-INPUT FORWARD ERROR CORRECTION DECODING



(57) **Abstract:** An apparatus for iterative hard-decision forward error correction decoding is described. A method comprises a binary receiver to convert an optical signal to an electrical signal, the electrical signal having a set of information symbols and a set of redundancy symbols, the set of redundancy symbols generated by different forward error correction (FEC) encoding schemes, and a first of a plurality of decoders coupled with the binary receiver and the plurality of decoders coupled together, each of the plurality of decoders to decode the set of information symbols with the set of redundancy symbols in accordance with the different FEC encoding schemes.

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Published:
— *with international search report*

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1 April 2004

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/09476

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03M13/29 H04L1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03M H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MIZUOCHI T ET AL: "Transparent Multiplexer featuring Super FEC for Optical Transport Networking" SUBOPTIC. THE INTERNATIONAL CONVENTION ON UNDERSEA COMMUNICATIONS, May 2001 (2001-05), pages 484-487, XP001151604 the whole document	1-35
X	EP 1 162 775 A (HITACHI LTD) 12 December 2001 (2001-12-12) the whole document	1-35

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
27 November 2003	05/12/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Farman, T

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/09476

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ARGON C ET AL: "TURBO PRODUCT CODES FOR PERFORMANCE IMPROVEMENT OP OPTICAL CDMA SYSTEMS" GLOBECOM'01. 2001 IEEE GLOBAL TELECOMMUNICATIONS CONFERENCE. SAN ANTONIO, TX, IEEE, NEW YORK, US, vol. 3 OF 6, 25 - 29 November 2001, pages 1505-1509, XP001054830 ISBN: 0-7803-7206-9 the whole document	1,3,5,11
X	YOUNG KIM, VINCENT POOR: "An optical CDMA packet network with turbo coding" 11TH IEEE INTERNATIONAL SYMPOSIUM ON PERSONAL INDOOR AND MOBILE RADIO , vol. 1, 18 - 21 September 2000, pages 751-756, XP010520734 the whole document	1,3,5,11
X	PUC A ET AL: "CONCATENATED FEC EXPERIMENT OVER 5000 KM LONG STRAIGHT LINE WDM TEST BED" OFC/IOOC '99: INTERNATIONAL CONFERENCE ON INTEGRATED OPTICS AND OPTICAL FIBER COMMUNICATION, SAN DIEGO, CA, US, 21 - 26 February 1999, pages THQ6-1-THQ6-4, XP000967046 ISBN: 0-7803-5430-3 the whole document	1,4
A	KAO M-S ET AL: "A PRODUCT-CODED WDM CODING SYSTEM" IEEE TRANSACTIONS ON COMMUNICATIONS, IEEE INC. NEW YORK, US, vol. 44, no. 1, 1996, pages 43-46, XP000549642 ISSN: 0090-6778 the whole document	1-35

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 03/09476

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1162775 A	12-12-2001	JP 2001358597 A	26-12-2001
		EP 1162775 A2	12-12-2001
		US 2001053225 A1	20-12-2001